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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GENACK, MATTHEW W	
ART UNIT	**PAPER NUMBER**
2645	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/936,290	MOLIERE, THOMAS	
	Examiner	Art Unit	
	Matthew W. Genack	2645	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meador *et. al.*, U.S. Patent No. 6,564,039 in view of Chabas, U.S. Patent No. 6,329,847, further in view of Butterfield, U.S. Patent No. 6,321,075, further in view of Pasternak, U.S. Patent No. 6,741,449.

Regarding Claims 1-2, Meador *et. al.* discloses a transceiver and method of operating said transceiver (Abstract, Column 1 Lines 6-9, Column 2 Lines 17-19, Column 3 Lines 53-54, Figs. 1-2). This transceiver includes a duplexer which allows said transceiver to simultaneously transmit and receive RF signals (Column 2 Lines 53-54). Meador *et. al.* teaches that the microcontroller of the transceiver preferably comprises a digital signal processor, said microcontroller having an input part (Column 3 Lines 43-45, Fig. 1). Said transceiver includes a plurality of mixers (Column Lines 45-50 and 55-61, Fig. 1). The mixer 140 of Figure 1 outputs an intermediate frequency (IF) signal (Column 7 Lines 58-61); after splitting and filtering, this signal is fed into the Tx modulation stage which processes this signal, thus the Tx modulation stage serves as the IF stage (Figs. 1-2). The Tx modulation stage (element 150 of Fig. 1 and the totality of Fig. 2) comprises a reference clock phase locked loop, 400, which in turn comprises

a phase detector, voltage controlled oscillator, and a frequency divider (Column 4 Lines 11-14, Fig. 2). Meador *et. al.* discloses the use of a programmable divider that uses an adjustable divider ratio for use with the reference clock phase locked loop (Column 5 Lines 10-16). A reference oscillator, 403, is used in conjunction with the reference clock phase locked loop (Column 5 Lines 10-16). Meador *et. al.* teaches the need to use the internal clock to generate timing signals for the data interfaces of the digital signal processing of a wireless communication device (Column 1 Lines 50-58), and in the specific invention, it is disclosed that the output of the reference clock, 161, is fed into the microcontroller, 110, which, as mentioned above, has a digital signal processor (Figs. 1-2). The frequency of the reference oscillator may be either approximately 16.8 MHz or approximately 26 MHz (Column 5 Lines 22-27). In the context of the application of the transceiver of the invention of Meador *et. al.* (cellular telephony), it is well known that channel bandwidths are typically less than 16.8 MHz.

Meador *et. al.* does not expressly disclose the use of a phase discriminator, nor the use of a digital clock synthesizer, nor the use of a digital tuning word.

Chabas discloses the use of a phase discriminator with a phase locked loop (Abstract, Column 2 Lines 19-31, Figs. 2-3).

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.* by using a phase discriminator in the reference clock phase locked loop.

One of ordinary skill in the art would have been motivated to make this modification because phase discriminators allow relatively fast synchronization between a variable oscillator and a reference frequency (Chabas, Column 1 Lines 26-34).

Neither Meador *et. al.* nor Chabas discloses the use of a digital clock synthesizer, nor the use of a digital tuning word.

Butterfield discloses the use of direct digital synthesis (DDS) for generating clock signals in a transceiver (Column 4 Lines 28-32 and 52-55, Fig. 2).

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.*, as modified by Chabas by providing for the clock signal with a clock synthesizer (supplied with input from the reference oscillator) that uses DDS.

One of ordinary skill in the art would have been motivated to make this modification because of the increased frequency accuracy and decreased cost of such an implementation.

Neither Meador *et. al.* nor Chabas nor Butterfield discloses the use of digital tuning words.

Pasternak discloses the use of an oscillator that is tuned with digital control words (Column 8 Lines 1-12, Fig. 5).

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.*, as modified by Chabas, as modified by Butterfield by providing digital words for tuning the reference oscillator.

One of ordinary skill in the art would have been motivated to make this modification because of the increased frequency accuracy and decreased cost of such an implementation.

Regarding Claims 3 and 6, every limitation of Claim 1 is disclosed by Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak. Furthermore, Meador *et. al.* discloses the use of a fractional N synthesizer in the transceiver (Column 4 Lines 34-42), and Butterfield discloses the use of a delta-sigma modulator in the transceiver (Abstract, Column 2 Lines 8-20).

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.*, as modified by Chabas, as modified by Butterfield, as modified by Pasternak by using a DDS synthesizer as the first frequency converter and including a delta-sigma modulator with the fractional N divider.

One of ordinary skill in the art would have been motivated to make this modification because of the increased frequency accuracy and decreased cost of such an implementation.

Regarding Claim 4, every limitation of Claim 1 is disclosed by Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak. Furthermore, Meador *et. al.* discloses the use of a control signal for the fine adjustment of the reference clock phase locked loop (Column 5 Lines 56-62).

Regarding Claims 5 and 10, every limitation of Claim 1 is disclosed by Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak.

Furthermore, Meador *et. al.* discloses the presence of a second phase locked loop with local oscillator, the LO PLL (435), and connected to a frequency divider (434), in the Tx Modulation Stage, which, as mentioned above, serves as the IF stage of the device (Fig. 2). Meador *et. al.* discloses the presence of a reference oscillator and Chabas discloses the use of a phase discriminator with a phase locked loop (see rejection of Claim 1). Meador *et. al.* discloses the use of a control signal for the fine adjustment of the reference clock phase locked loop (see rejection of Claim 4). Meador *et. al.* discloses the presence of a baseband I/Q modulation stage (436) that transmits analog I and Q signals to the Tx up-converter stage (Column 4 Lines 1-7 and 29-33, Fig. 2). Finally, Meador *et. al.* discloses the presence of several mixers and oscillators in the Tx Modulation Stage.

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.*, as modified by Chabas, as modified by Butterfield, as modified by Pasternak by providing a phase discriminator with the second phase locked loop, said phase discriminator receiving input from the oscillators of the first and second phase locked loops and from the outputs of a mixer and transmission oscillator in the Tx Modulation Stage.

One of ordinary skill in the art would have been motivated to make this modification because phase discriminators allow relatively fast synchronization between a variable oscillator and a reference frequency (Chabas, Column 1 Lines 26-34).

Regarding Claims 7-8, every limitation of Claim 1 is disclosed by Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak. Furthermore,

Meador *et. al.* discloses that the reference oscillator signal is fed into the frequency divider of reference clock phase locked loop before being used by said phase locked loop (*e.g.*, the first phase locked loop) (Fig. 2).

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak, further in view of Jakobsson, U.S. Patent No. 6,246,867.

Every limitation of Claim 1 is disclosed by Meador *et. al.* in view of Chabas, further in view of Butterfield, further in view of Pasternak.

Neither Meador *et. al.*, nor Chabas, nor Butterfield, nor Pasternak expressly discloses the use of a homodyne receiver.

Jakobsson discloses a homodyne receiver that comprises an antenna, two filters, three amplifiers, two mixers, two analog-to-digital converters, a phase shifter, and a local oscillator (Column 6 Lines 59-67, Figs. 2-3).

At the time that the invention was made, it would have been obvious to one of ordinary skill in the art to modify the invention of Meador *et. al.*, as modified by Chabas, as modified by Butterfield, as modified by Pasternak by using a homodyne receiver and inputting the received RF modulated carrier signal (from the antenna) and the output signal of the first local oscillator into the reception mixer so as to down-convert the received RF signal to baseband.

One of ordinary skill in the art would have been motivated to make this modification because homodyne receivers use an intermediate frequency of zero hertz,

or DC, and the information signal formerly modulated onto the RF signal is thus all that remains (Column 5 Lines 26-27).

Response to Arguments

3. Applicant's arguments, filed 20 July 2005, with respect to the 35 USC 112, second paragraph, rejection of Claim 1 have been fully considered and are persuasive. The 35 USC 112, second paragraph, rejection of Claim 1 has been withdrawn.

4. Applicant's arguments filed 20 July 2005, with respect to the 35 USC 103 rejections, have been fully considered but they are not persuasive. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action. Thus, at present, the effective date remains 1 March 2000.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Genack whose telephone number is 571-272-7541. The examiner can normally be reached on FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fan Tsang can be reached on 571-272-7547. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Genack

Examiner

Art Unit 2645

Matthew Genack

4 October 2005

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